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09/766,846	01/23/2001	Hiroki Shinkawata	50090-275	1557

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EXAMINER
VU, HUNG K

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 08/04/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/766,846	SHINKAWATA, HIROKI	
	Examiner	Art Unit	
	Hung K. Vu	2811	

-- The MAILING DATE of this communication app ars on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 May 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) *16-20* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,5-7,9-11 and 13-15* is/are rejected.

7)☒ Claim(s) *3,4,8 and 12* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Objections

1. Claims 2 and 3 are objected to because of the following informalities:

In claim 2, line 13, delete "a" before the phrase "capacitor contact plugs" for clarity.

In claim 3, line 3, "the surface" should be changed to "a surface" for clarity.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

Claim 1 is rejected under 35 U.S.C. 102(a) as being anticipated by Harvey (PN 6,174,803).

Harvey discloses, as shown in Figure 25, a semiconductor device comprising,

conductive transfer gates (214) comprising conductive parts (239);

contact plugs (239) adjacent to the conductive transfer gates, each contact plug and each conductive transfer gate having a respective upper surface, wherein the upper surfaces of the contact plugs and the upper surfaces of the conductive transfer gates are substantially coplanar;

each conductive transfer gate having a gate insulating film,

a gate electrode layer (217), and side walls (219) for covering sides of the gate insulating film and the gate electrode;

a first interlayer insulating film (222) having a surface which defines the same surface as the upper surfaces as the upper surfaces of the conductive parts of the transfer gates and the contact plugs;

a second interlayer insulating film (260,262) formed on the first interlayer insulating film;

diameter-reduced contact plugs (263) which are smaller than the contact plugs and extend through the second interlayer insulating film to conduct to the contact plugs, respectively.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-2 and 13-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sung (PN 6,137,130, of record) in view of Yang et al. (PN 6,329,232).

Sung discloses, as shown in Figures 4A-4B and 6B, a semiconductor device comprising,

conductive transfer gates (44) comprising conductive parts (4);

contact plugs (50) adjacent to the conductive transfer gates, each contact plug and each conductive transfer gate having a respective upper surface, wherein the upper surfaces of the contact plugs and the upper surfaces of the conductive transfer gates are substantially coplanar;

each conductive transfer gate having a gate insulating film (3),

a gate electrode layer (4), and side walls (7) for covering sides of the gate insulating film and the gate electrode;

a first interlayer insulating film having a surface which defines the same surface as the upper surfaces as the upper surfaces of the conductive transfer gates and the contact plugs;

a second interlayer insulating film (12) formed on the first interlayer insulating film;

diameter-reduced contact plugs (13) which are smaller than the contact plugs and extend through the second interlayer insulating film to conduct to the contact plugs, respectively. Note attached red-line Figure 4B of Sung.

Sung does not disclose the upper surfaces of the contact plugs and the upper surfaces of the conductive parts of the transfer gates are substantially coplanar. However, Yang et al. discloses the upper surfaces of the contact plugs and the conductive parts of the transfer gate are substantially coplanar. Note Figure 1D of Yang et al.. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the device of Sung having the upper surfaces of the contact plugs and the conductive parts of the transfer gate are substantially coplanar, such as taught by Yang et al. in order to reduce the overall thickness of the device, to prevent the two adjacent gate electrodes from being shorted, to form a plug contact having a small size so that more many cells can be implement in a same chip area.

With regard to claim 2, Sung and Yang et al. discloses the device further including a memory cell section (DRAM cell) having a plurality of memory cells,

the memory cell section including, in addition to the conductive transfer gates, the contact plugs, and the first and second interlayer insulating films,

a bit line (14) formed on the second interlayer insulating film;

a third interlayer insulating film (52) formed on the second interlayer insulating film so as to cover the bit line;

capacitors (55) formed on the third interlayer insulating film;

the memory cell section further including, as the diameter-reduced contact plugs, which include

a bit line contact plug which extends through the second interlayer insulating film to bring the contact plugs and the bit line into conduction;

capacitor contact plugs which extend through the second and third interlayer insulating films to bring the contact plugs and the capacitor into conduction.

With regard to claim 13, Sung discloses claimed invention substantially as claimed including the semiconductor device as recited in the rejection above. Sung does not disclose the gate electrode layer has a metal layer and a barrier metal which surrounds the metal layer. However, Yang et al. discloses the gate electrode layer has a metal layer (110) and a barrier metal (108,109) which surrounds the metal layer. Note Figure 1D of Yang et al.. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the gate electrode layer of Sung having a metal layer and a barrier metal which surrounds the metal layer, such as taught by Yang et al. because metal gate has a low sheet resistance so that the word line delay is effectively reduced.

With regard to claims 14 and 15, Sung and Yang et al. disclose the gate insulating film of the conductive transfer gate is silicon oxide. Note that the terms "a CVD insulating film formed by a CVD method" and "a thermal oxide film formed by a thermal oxidation method or a thermally-oxidized nitride film formed by a thermal oxidation nitriding method" are method recitations in a device claimed. Note that only the final product is relevant, not the method of making. A product by process claim is directed to the product per se, no matter how actually made. See also MPEP 2113. Moreover, an old or obvious product produced by a new method is not a patentable product, whether claimed in "product by process" claims or not.

4. Claims 5 – 6 and 9 – 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sung (PN 6,137,130, of record) in view of Yang et al. (PN 6,329,232) and further in view of Ozaki et al. (PN 6,104,052, of record).

With regard to claims 5 and 9, Sung and Yang et al. disclose claimed invention substantially as claimed including the semiconductor device as recited in the rejection above. Sung and Yang et al. further disclose the semiconductor device is a DRAM device. Sung and Yang et al. do not disclose the device further includes a logic circuit section, wherein the logic circuit section including a plurality of transistors, in addition to the transfer gates, the contact plugs, and the first and second interlayer insulating films, bit lines formed on the second interlayer insulating films, diameter-reduced contact plugs. Note that it is well-known that the DRAM device includes memory section and a peripheral circuit (or logic circuit) section. However, Ozaki et al. discloses DRAM device comprises includes memory section and a logic circuit section, wherein the logic circuit section including a plurality of transistors (19b), in addition to the transfer gates,

the contact plugs (47), and the first and second interlayer insulating films (22a,22b), bit lines (29b) formed on the second interlayer insulating films, diameter-reduced contact plugs (27b). Note Figure 14G of Ozaki et al.. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the device of Sung and Yang et al. having a logic circuit section, wherein the logic circuit section including a plurality of transistors, in addition to the transfer gates, the contact plugs, and the first and second interlayer insulating films, bit lines formed on the second interlayer insulating films, diameter-reduced contact plugs, such as taught by Ozaki et al. in order to control the memory circuit section to perform the desire function (by switching and providing power, filter, rectify, etc.).

With regard to claims 6 and 10, Sung, Yang et al. and Ozaki et al. disclose the logic circuit section has NMOS transistors and PMOS transistors both of which constitute CMOS transistors. (Note Col. 21, line 36 – Col. 22, line 5 of Ozaki et al.)

5. Claims 7 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sung (PN 6,025,227, of record) in view of Yang et al. (PN 6,329,232) and Ozaki et al. (PN 6,104,052, of record) and further in view of Hsu et al. (PN 5,693,974, of record).

Sung, Yang et al. and Ozaki et al. disclose claimed invention substantially as claimed including the semiconductor device as recited in the rejection above. Sung, Yang et al. and Ozaki et al. further disclose contact plugs provided in association with NMOS transistors have a doped silicon layer containing an N-type impurity, and contact plugs provided in association with PMOS transistors have a doped silicon layer containing an P-type impurity. Sung, Yang et al.

and Ozaki et al. do not disclose gate electrode layers of NMOS transistors have a doped silicon layer containing N-type impurity and gate electrode layers of PMOS transistors have a doped silicon layer containing P-type impurity. However, Hsu et al. discloses a gate electrode layer (18) of NMOS transistor has a doped silicon layer containing N-type impurity (arsenic) and a gate electrode layer (18) of PMOS transistor has a doped silicon layer containing P-type impurity (boron). Note Figures 9 – 10 and Col. 4, lines 31 – 46 of Hsu et al.. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the device of Sung, Yang et al. and Ozaki et al. having gate electrode layers of NMOS transistors have a doped silicon layer containing N-type impurity and gate electrode layers of PMOS transistors have a doped silicon layer containing P-type impurity, such as taught by Hsu et al. in order to increase the gate conductivity and to improve the work function of transistors.

Allowable Subject Matter

6. Claims 3-4, 8 and 12 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

7. The following is an examiner's statement of reasons for allowance:

Applicant's claims 3-4, 8 and 12 are allowable over the references of record because none of these references disclose or can be combined to yield the claimed invention such as the contact plug corresponding to the bit line has a doped silicon layer containing an impurity and a silicide film formed only at a portion brought into contact with the bit line contact plug, and the bit line contact plug has a barrier metal brought into contact with each contact plug and a metal

layer formed on the barrier metal, as recited in claim 3; each contact plug provided in association with NMOS transistor has a doped silicon layer containing an N-type impurity, each contact plug provided in association with the PMOS transistor has a doped silicon layer containing a P-type impurity, and any of gate electrode layers in association with the NMOS transistors and gate electrode layers provided in association with the PMOS transistors has a doped silicon layer containing the first conduction type impurity, as recited in claim 8; and contact plugs and gate electrode layers respectively have a doped silicon layer containing an impurity and a silicide film for covering the surface of the doped silicon layer, and each diameter-reduced contact plug has a barrier metal brought into contact with the silicide film, and a metal formed on the barrier metal, as recited in claim 12.

Response to Arguments

8. Applicant's arguments with respect to claim 1 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after

the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hung K. Vu whose telephone number is (703) 308-4079. The examiner can normally be reached on Mon-Thurs 6:00-3:30, alternate Friday 7:00-3:30, Eastern Time.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (703) 308-2772. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Tom Thomas

Vu

July 24, 2003

TOM THOMAS
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